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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/556,398	11/10/2005	Francois Droz	90500-000067/US	6278

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EXAMINER	
MAI, THIEN T	
ART UNIT	PAPER NUMBER
2887	
MAIL DATE	DELIVERY MODE
02/04/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/556,398	DROZ, FRANCOIS	
	Examiner	Art Unit	
	Thien T. Mai	2887	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 November 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 November 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 11/19/2008 has been entered.

Objections

Claim 3 line 1: "the layer" lacks antecedent basis. Please clarify which (i.e. in claim 1 or

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 3 calls for the layer of insulation material having a cavity for the chip to be inserted while in claim 1 recites that the layer is applied on the electronic component thus it is unclear which is the layer of insulation material claimed.

3. Claim 6 recites "the cavity of the electronic component"; however, the claim limitations in claim 6 and parent claim 1 do not clearly define as to whether the component having a cavity. The preamble of claim 1 merely says "electronic component made up of a chip provided with contacts on one of the faces of the chip"

and the claim limitations in claim 1 reciting the [entire] component into a cavity of the substrate. Thus it is unclear whether the component having a cavity.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim(s) 1-3, 9-11 is/are rejected under 35 U.S.C. 103(a) as being unpatentable over *Halope* (US 6,851,618)

Halope discloses the subject matter for the following claims:

Re claim 1, *Halope* teaches a process for assembling at least one electronic component made up of a chip provided with contacts on one of the faces of the chip, said contacts being set off on a conductive film constituting flat conductive areas that extend the contacts of the chip in a plane over the chip, the conductive areas are being connected to conductive tracks placed on a surface of a planar insulating substrate, comprising:

placing the substrate on a work surface, the face including conductive tracks 18, 62, 64 (Fig. 1, 4-5) being oriented upwards, placing the electronic component 40 (made up of a chip 26 on a double sided circuit 10 – see Fig. 2, col. 3 lines 18-25) into a cavity of the substrate situated in a zone including the conductive tracks 62, 64, 18, the chip being inserted into the cavity, the conductive areas of the electronic component coming into contact with the corresponding conductive tracks of the substrate, and

applying a layer of insulating material which extends concurrently on the electronic component and at least on the zone of the substrate surrounding said electronic component, wherein the conductive areas of the electronic component and the conductive tracks of the substrate are in contact to achieve an electric connection via a pressure of application of the insulating material layer on the electronic component, and configured to rub together when repeated stressed are exerted on the substrate (col. 4 lines 19-38: electronic component 40 contacts are in connection with antenna without using glue and Fig. 4-6 show the double sided circuit portions of the component 40 are in contact with antenna portions 62, 64 and insulating material covers the entire electronic component 40 and its surrounding; although not expressly described, it would have been obvious that at least a small rubbing/friction would occur at the chip contacts with the antenna while repeated stresses are exerted due to pressure on the electronic component and hot injection of fluid(s)).

Re claim 2, *Halope* teaches the electronic component is coated by an insulating material on the face of the chip opposite to the face provided with contacts (see glue 34, 36 in Fig. 2).

Re claim 3, *Halope* discloses the layer of insulating material is made up of a first substrate 58 including a cavity into which the chip of the electronic component is inserted, the conductive areas of said electronic component being applied against the surface of the first substrate 58 (Fig. 5) connecting to corresponding conductive surfaces of a second substrate (substrate 58 is on substrate 38) placed on the work surface

Re claim 9, *Halope* teaches the cavity of the electronic component is formed by milling or by stamping a window (col. 3 lines 18+).

Re claim 11, *Halope* teaches the electronic component is made up of a module including a set of flat contacts on one of the faces of the module, each contact of the set being linked with a contact area on the opposite face (see abstract, col. 2 lines 46-50 *Halope* teaches hybrid contact-contactless smart card, which inherently known to include an upper face in direct physical contact with a reader as well as including a non-contact interface through antenna).

5. Claim(s) 6 is/are rejected under 35 U.S.C. 103(a) as being unpatentable over *Halope* (US 6,851,618) in view of *Ikeda* (JP 01020197 A). *Halope*'s teachings have been discussed above.

Halope is unclear with respect to heating the chip before inserting into the cavity.

Ikeda discloses the electronic component is obtained by heating the chip of the electronic component with a mold section 9 resulting in heat dissipation before inserting into the cavity along with aluminum foils 4 (Fig. 1-2, see abstract).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of *Ikeda* for achieving better productivity and production speed by inserting the component into the cavity after being molded while still being warm resulted from the heated mold.

6. Claim(s) 12-14 is/are rejected under 35 U.S.C. 103(a) as being unpatentable over *Halope* (US 6,851,618) in view of *Fischer et al.* (US 5969951 A). *Halope*'s teachings have been discussed above.

Re claim 12, *Halope* teaches a hybrid embodiment in Fig. 1 showing first substrate 22 having a cavity window into which the module is inserted. The flat contact shows on the surface level of the first substrate. *Halope* teaches in Fig. 5 a contactless embodiment where there is a conductive contact between the opposite face of the module and a portion of the substrate.

Halope is silent with respect to a second substrate and there is a conductive contact between the opposite face of the module and the second substrate.

Fischer et al. discloses a multi-layer hybrid card having a flat contact shows on the surface level of a first substrate. *A* conductive contact exists between the opposite face of the module and a second substrate (Fig. 1, 6-10 show the module 3 having a face contact shows on a first substrate (Fig. 1) and its opposite face conductively contacts/leans against the surface of a second substrate assembled on the first substrate (i.e. the second substrate is on the first when viewed upside down)

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of *Fischer et al.* to further gain more flexibility for the amount of layers in the card.

Re claim 13, *Halope* discloses at least one module is mounted in one of the substrates, said module including conductive areas connected by pressure on the corresponding conductive tracks of either of the substrates (*Halope* - col. 1 lines 28-35, col. 1 line 53-60, col. 3 lines 7-17).

Re claim 14, *Halope* discloses a supplementary step of gluing and pressing the assembly formed by the superposition of the substrates (*Halope* - col. 1 lines 28-35, col. 1 line 53-60, col. 3 lines 7-17).

Remarks

Applicant's arguments have been considered but are moot in view of the new ground(s) of rejection.

Further, In response to applicant's argument that the contact surfaces cannot rub together, it is respectfully submitted that since the contacts as seen in the figures 2 and 5 the area of the contacts are substantial and movable since conductive glue is not needed at the contact before the hot lamination under pressure which would been obvious to an artisan that it would cause at least some movement of the component inside the cavity.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thien T. Mai whose telephone number is 571-272-8283. The examiner can normally be reached on Monday through Friday, 8:00 - 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steve S. Paik can be reached on 571-272-2404. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Thien T Mai/
Examiner, Art Unit 2887

/EDWYN LABAZE/
Primary Examiner, Art Unit 2887